LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A semiconductor device comprising:

a semiconductor die having a pad-mounting surface defining a horizontal plane, and a plurality of spaced apart first bonding pads formed on said pad-mounting surface; and

a multi-level interconnect structure formed on said pad-mounting surface, and including

a first insulating layer formed on said pad-mounting surface and formed with a plurality of first holes, each of which exposes a respective one of said first bonding pads from said pad-mounting surface,

a plurality of first level conductive horizontal bodies, each of which has an end section that fills a respective one of said first holes to electrically connect with a respective one of said first bonding pads, and an extension that extends from said end section, that is formed on said first insulating layer, and that has a connecting end horizontally offset from the respective one of said first holes,

a second insulating layer formed on said first insulating layer and formed with a plurality of first holes, each of which exposes said connecting end of said extension of a respective one of said first level conductive horizontal bodies from said second insulating layer, and

a plurality of second level conductive vertical bodies, each of which fills a respective one of said first holes in said second insulating layer to electrically connect with said connecting end of said extension of a respective one of said first level conductive horizontal bodies, and each of which has a connecting end that extends through the respective one of said first holes in said second insulating layer.

2. (Original) The semiconductor device of Claim 1, further comprising a third insulating layer formed on said second insulating layer and formed with a plurality of first holes, said connecting end of each of said second level conductive vertical bodies extending into a respective one of said first holes in said third insulating layer.

3. (Original) The semiconductor device of Claim 2, further comprising a plurality of conductive bumps, each of which extends into a respective one of said first holes in said third insulating layer, and each of which is electrically connected to said connecting end of a respective one of said second level conductive vertical bodies.

4. (Original) The semiconductor device of Claim 1, wherein said semiconductor die further has a plurality of spaced apart second bonding pads formed on said pad-mounting surface, said first insulating layer being further formed with a plurality of second holes, each of which exposes a respective one of said second bonding pads from said first insulating layer, said semiconductor device further comprising a plurality of first level conductive vertical bodies, each of which fills a respective one of said second holes in said first insulating layer to electrically connect with a respective one of said second bonding pads, and each of which has a connecting end that extends through the respective one of said second holes in said first insulating layer.

5. (Original) The semiconductor device of Claim 4, wherein said second insulating layer is further formed with a plurality of second holes, each of which exposes said connecting end of a respective one of said first level conductive vertical bodies from said second insulating layer, said semiconductor device further comprising a plurality of second level conductive horizontal bodies, each of which has an end section that fills a respective one of said second holes in said second insulating layer to electrically connect with said connecting end of a respective one of said first level conductive vertical bodies, and an extension that extends from said end section of a respective one of said second level conductive horizontal bodies, that is formed on said second insulating layer, and that has a connecting end horizontally offset from the respective one of said second holes in said second insulating layer.

6. (Original) The semiconductor device of Claim 5, further comprising a third insulating layer formed on said second insulating layer and formed with a plurality of first and second holes, said connecting end of each of said second level conductive vertical bodies extending into a respective one of said first holes in said third insulating layer, said connecting end of said

extension of each of said second level conductive horizontal bodies extending into a respective one of said second holes in said third insulating layer.

7. (Original) The semiconductor device of Claim 6, further comprising a plurality of first and second conductive bumps, each of said first conductive bumps extending into a respective one of said first holes in said third insulating layer to electrically connect with said connecting end of a respective one of said second level conductive vertical bodies, each of said second conductive bumps extending into a respective one of said second holes in said third insulating layer to electrically connect with said connecting end of said extension of a respective one of said second level conductive horizontal bodies.

8. (Original) The semiconductor device of Claim 7, further comprising a first metal layer that is formed on a respective one of said first bonding pads and that is disposed within a respective one of said first holes in said first insulating layer, each of said first level conductive horizontal bodies including a conductive paste layer that has a first portion extending from said first metal layer, and a second portion formed on said first insulating layer, and a second metal layer formed on and cooperating with said second portion of said conductive paste layer to define said extension of the respective one of said first level conductive horizontal bodies.

9. (Withdrawn) A method for making a semiconductor device that includes a semiconductor die having a pad-mounting surface defining a horizontal plane and a plurality of first bonding pads formed on the pad-mounting surface, the method comprising the steps of:

forming a first insulating layer on the pad-mounting surface;

forming a plurality of first holes in said first insulating layer, each of said first holes exposing a respective one of the first bonding pads from said first insulating layer;

forming a plurality of first level conductive horizontal bodies, each of which has an end section that fills a respective one of said first holes to electrically connect with a respective one of the first bonding pads, and an extension that extends from said end section, that is formed on

said first insulating layer, and that has a connecting end horizontally offset from the respective one of said first holes;

forming a second insulating layer on said first insulating layer;

forming a plurality of first holes in said second insulating layer, each of said first holes in said second insulating layer exposing said connecting end of said extension of a respective one of said first level conductive horizontal bodies; and

forming a plurality of second level conductive vertical bodies, each of which is electrically connected to said connecting end of said extension of a respective one of said first level conductive horizontal bodies, each of which fills a respective one of said first holes in said second insulating layer, and each of which has a connecting end that extends through the respective one of said first holes in said second insulating layer.

10. (Withdrawn) The method of Claim 9, further comprising forming a third insulating layer on said second insulating layer, and forming a plurality of first holes in said third insulating layer such that said connecting end of each of said second level conductive vertical bodies extends into a respective one of said first holes in said third insulating layer.

11. (Withdrawn) The method of Claim 10, further comprising forming a plurality of conductive bumps, each of which extends into a respective one of said first holes in said third insulating layer, and each of which is electrically connected to said connecting end of a respective one of said second level conductive vertical bodies.

12. (Withdrawn) The method of Claim 9, the semiconductor die further having a plurality of spaced apart second bonding pads formed on the pad-mounting surface, further comprising:

forming a plurality of second holes in said first insulating layer, each of said second holes in said first insulating layer exposing a respective one of the second bonding pads from said first insulating layer; and

forming a plurality of first level conductive vertical bodies, each of which fills a respective one of said second holes in said first insulating layer to electrically connect with a respective one of the second bonding pads, and each of which has a connecting end that extends through the respective one of said second holes in said first insulating layer.

13. (Withdrawn) The method of Claim 12, further comprising:

forming a plurality of second holes in said second insulating layer, each of said second holes in said second insulating layer exposing said connecting end of a respective one of said first level conductive vertical bodies from said second insulating layer; and

forming a plurality of second level conductive horizontal bodies, each of which has an end section that fills a respective one of said second holes in said second insulating layer to electrically connect with said connecting end of a respective one of said first level conductive vertical bodies, and an extension that extends from said end section of a respective one of said second level conductive horizontal bodies, that is formed on said second insulating layer, and that has a connecting end horizontally offset from the respective one of said second holes in said second insulating layer.

14. (Withdrawn) The method of Claim 13, further comprising forming a third insulating layer on said second insulating layer, and forming a plurality of first and second holes in said third insulating layer such that said connecting end of each of said second level conductive vertical bodies extends into a respective one of said first holes in said third insulating layer, and that said connecting end of said extension of each of said second level conductive horizontal bodies extends into a respective one of said second holes in said third insulating layer.

15. (Withdrawn) The method of Claim 14, further comprising forming a plurality of first and second conductive bumps such that each of said first conductive bumps extends into a respective one of said first holes in said third insulating layer to electrically connect with said connecting end of a respective one of said second level conductive vertical bodies, and that each of said second conductive bumps extends into a respective one of said second holes in said third

insulating layer to electrically connect with said connecting end of said extension of a respective one of said second level conductive horizontal bodies.

16. (New) A semiconductor device comprising:

a semiconductor die having a pad-mounting surface defining a horizontal plane, and a plurality of spaced apart first and second bonding pads formed on said pad-mounting surface; and

a multi-level interconnect structure formed on said pad-mounting surface, and including

a first insulating layer formed on said pad-mounting surface,

a plurality of first level conductive horizontal bodies, each of which extends from a respective one of said first bonding pads through said first insulating layer, and each of which has one end connected to a respective one of said first bonding pads, and an opposite end that is offset from the respective one of said first bonding pads, and

a plurality of first level conductive vertical bodies, each of which extends in a direction normal to the horizontal plane from a respective one of said second bonding pads through said first insulating layer, and each of which has one end connected to a respective one of said second bonding pads, and an opposite end that is aligned with the respective one of said second bonding pads in said normal direction;

wherein each of said first level conductive vertical bodies has a projecting area, projected on the horizontal plane, that is disposed within a boundary of the respective one of said second bonding pads.

17. (New) The semiconductor device of Claim 16, wherein said multi-level interconnect structure further includes a second insulating layer formed on said first insulating layer, and a plurality of second level conductive vertical bodies, each of which extends through said second insulating layer, and each of which has one end connected to said opposite end of a respective one of said first level conductive horizontal bodies, and an opposite end that is aligned with said opposite end of the respective one of said first level conductive horizontal bodies in said normal direction.

18. (New) The semiconductor device of Claim 17, wherein said multi-level interconnect structure further includes a plurality of second level conductive horizontal bodies, each of which extends through said second insulating layer, and each of which has one end connected to said opposite end of a respective one of said first level conductive vertical bodies, and an opposite end that is offset from said opposite end of the respective one of said first level conductive vertical bodies.

19. (New) The semiconductor device of Claim 18, wherein said multi-level interconnect structure further includes a third insulating layer formed on said second insulating layer, said opposite end of each of said second level conductive vertical bodies extending into said third insulating layer.

20. (New) The semiconductor device of Claim 19, further comprising a plurality of first and second conductive bumps, each of said first conductive bumps extending into said third insulating layer to electrically connect with said opposite end of a respective one of said second level conductive vertical bodies, each of said second conductive bumps extending into said third insulating layer to electrically connect with said opposite end of a respective one of said second level conductive horizontal bodies.